ACM MEDEA Workshop

MEmory performance:
DEaling with Applications, systems and architecture

held in conjunction with PACT 2008 Conference

http://garga.iet.unipi.it/medea08/

"*Medea (memory) helps Jason (processor). Will Medea kill Jason's sons?*"

PACT-2008
Toronto, Canada
October 25-29, 2008

Call for Papers

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MEDEA-2008 aims to continue the high level of interest of the previous editions held with PACT Conference since 2000.

Due to the ever-increasing gap between CPU and memory speed, there is always great interest in evaluating and proposing processor, multiprocessor, CMP, multi-core and system architectures dealing with the "memory wall" and wire-delay problems. At the same time, a modular high-level design is becoming more and more attracting in order to reduce design costs. In this scenario, design solutions and their corresponding performance are shaped by the combined pressure of a) technological opportunities and limitations, b) features and organization of system architecture and c) critical requirements of specific application domains. Evaluating and controlling the effects on the memory subsystem (e.g. caches, interconnection, bus, memory, coherence) of any architectural proposal is extremely important both from the performance and power points of view. In particular, the emerging trend of single-chip multi-core solutions, will push towards new design principles for memory hierarchy and interconnection networks, especially when the design is aimed to build systems with a high number of cores, which aim to scale performance and power efficiency in a variety of application domains. From a slightly different point of view, the mutual interaction between the application behavior and the system on which it executes, is responsible of the figures of merit of the memory subsystem and, therefore, pushes towards specific solutions. Typical architectural choices of interest include, single processors, chip multiprocessors, SoC, tiled/clustered architectures, multithreaded or VLIW architectures, massive parallelism designs, heterogeneous architectures, architectures equipped with application-domain accelerators as well as endowed with reconfigurable modules. The emerging network on chip infrastructure and transactional memory may suggest new solutions and issues.

MEDEA Workshop wants to continue to be a forum for academic and industrial people to meet, discuss and exchange their ideas and experience in the design and evaluation of architectures for embedded, commercial and general/special purpose systems taking into account memory issues. Proceedings of the Workshop will be published under **ACM ISBN** and will appear in **ACM DL**. As in the previous years, a selection of papers will be considered for publication on **Transactions on HIPEAC** (http://www.hipeac.net/journal). The format of the workshop includes the presentation of selected papers and discussion after each presentation.

Topics of Interest:
- Memory hierarchy design, analysis, tuning for embedded, general and special purpose systems
- On-chip Multiprocessors and System On Chip architectures, development tools and applications
- Issues in memory hierarchy design of scalable single chip systems
- Memory hierarchy issues for heterogeneous and accelerator-based systems
- Low-Power/Wire Delay design of memory hierarchies
- Inter-Chip and Intra-Chip memory latency tolerant and reduction techniques
- Cache coherence and memory models
- Exploitation of application parallelism (e.g.: ILP, TLP, DLP)
- Transactional Memory
- Compile/link time optimization techniques
- Network On Chip
- Academic/industrial experience in high performance, embedded systems and memory design

Information for Authors - Dates

The papers should be 6-8 pages in length. The abstracts and papers should be submitted in PDF format by email to Pierfrancesco Foglia and Sandro Bartolini. Paper should be written in standard ACM SIG Proceedings Template. Please email submissions by August, 7th 2008. Authors will be notified of acceptance or rejection by September, 21st 2008 and the final papers are due by September, 28th 2008.

To speed-up the reviewing process, we encourage also submission of abstract by July 31st, 2008.

July 31, 2008	Abstract Submission (not mandatory)
August 07, 2008	Paper Submission Deadline
September 21, 2008	Notification of Acceptance
September 28, 2008	Final Papers Due
October 25-26, 2008	MEDEA-2008 Workshop held in PACT (to be defined)