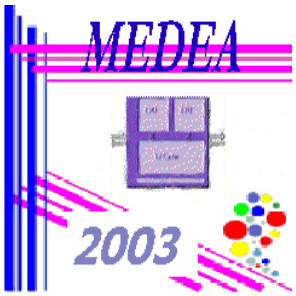

MEDEA Workshop

MEmory performance:
DEaling with Applications, systems and architecture

held in conjuction with PACT 2003 Conference
Sept. 27- Oct. 1, 2003, New Orleans, Louisiana, USA

http://garga.iet.unipi.it/medea03/

"*Medea helps Jason. Will Medea kill Jason's sons?*"

ACM SIGARCH

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Call for Papers

MEDEA-2003 aims to continue the high level of interest in the first three MEDEA Workshops held with PACT'00, PACT'01 and PACT'02.
Due to the ever-increasing gap between CPU and memory speed, there is a great interest in evaluating and proposing processor, multiprocessor and system architectures dealing with the "memory wall" problem.
In this scenario, memory performance issues can be better addressed when considering system architecture and application domain in a joint manner. In fact, it is the combined effect of the applications and the system on which they are executing that stresses the memory subsystem and pushes towards specific solutions.
Typical architectural choices include single processor vs. multiprocessor solutions, single chip vs. COTS design, superscalar, multithreaded or VLIW architectures. Application domains encompass commercial (Web, DB, e-business, and multimedia), embedded (personal, mobile, automotive, automation and medical), networking applications, etc.

The MEDEA-2003 Workshop wants to be a forum for academic and industrial people to meet, discuss and exchange their ideas and experience on the design and evaluation of architectures for embedded, commercial and general purpose systems. Main topics are memory performance issues and solutions in the various application domains.
As in the previous editions, accepted papers, in an extended form if needed, will appear on the March 2004 special issue of "ACM SigArch Computer Architecture News".

The format of the workshop includes presentations of selected papers and discussion after each presentation.

Topics of Interest

- Memory Hierarchy Design for Embedded Systems
- Memory Hierarchy Design for Commercial/Scientific/General Purpose Applications
- Processor and System Architecture and their impact on memory performances
- Cache memory: Organization and Coherence
- Bus/Interconnection Architecture
- Low-Power design of memory hierarchies
- Operating system memory management and virtual memory systems
- On-chip Multiprocessors and System On Chip
  - architectures, development tools, applications and optimizations
  - solutions for embedded, commercial, scientific and technical workloads
  - power consumption and performance evaluation
- Academic/industrial experience in
  - high performance, general purpose, embedded systems and memory design
- Multithreaded applications
- Code optimization techniques
- Memory Access Decoupling
- Latency Tolerance and Reduction techniques
- Instruction and Thread Level Parallelism
- Workload characterization

Important Dates

June 8, 2003	Abstract Submission (not mandatory)
June 16, 2003	Paper Submission Deadline
July 14, 2003	Notification of Acceptance
September 1, 2003	Final Papers Due
September 27, 2003	Start of MEDEA-2003 Workshop

Information for Authors

The papers should be at most 8 pages in length. The abstracts and papers should be submitted in either postscript or PDF format by email to the workshop-organizing members: Pierfrancesco Foglia and Sandro Bartolini.
Paper should be written in standard IEEE format for conference proceedings. Hard copy (postal) submissions will NOT be accepted. To speed-up the reviewing process, we encourage also submission of abstract by June 8, 2003.